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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,835	KOGA, SHOUICHI	
	Examiner	Art Unit	
	EBONI GILES	4133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy of Japanese Patent No. 2004-098926, filed on March 30, 2004, has been received in this National Stage Application PCT/JP2005/004412, filed on March 8, 2005, from the International Bureau.

Information Disclosure Statement

2. The information disclosure statement (IDS) PTO-1449 submitted on 1/17/06 was filed before the mailing date of the non-final office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 11, 14, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0121753 to Sugar et al ('753 publication) and in view of U.S. Patent Publication 2004/0242183 to Sugar et al ('183 publication).

As to Claim 1, the "753" publication discloses "a receiver comprising: a plurality of receiver branches operable to receive signals," where the radio

transceiver 10 is suitable for processing radio frequency signals detected by at least two antennas. The foregoing description is directed to an embodiment with two antennas 12 and 14, and an associated transmit and receive path for each, but this same architecture can be generalized to support in general N processing paths for N-antennas [¶ 0025] and further discloses that the receiver comprises receiver circuits 20 and 30. There is a receiver circuit 20 for antenna 12 and a receive circuit or section 30 for antenna 14 [¶ 0027, Fig. 1];

The '753 publication further discloses "a plurality of sample-and-hold circuits, each of which is connected to corresponding one of said plurality of receiver branches, each of said plurality of sample-and-hold circuits," where each receiver circuit 20 and 30 includes a…sample-and-hold circuit 28 [¶ 0027, Fig. 1];

The '753 publication further discloses "a switch connected to said plurality of sample-and-hold circuits," where a front-end section 90 couples the radio transceiver 10 to antennas 12 and 14. There are switches 62 and 64 coupled to antennas 12 and 14, respectively. Switch 62 selects whether the output of the transmit circuit 60 or the input to the receiver circuit 20 is coupled to antenna 12 [¶ 0028, Fig. 1];

The '753 publication further discloses "a demodulating unit connected to said switch, said demodulating unit being operable to demodulate data from output signals from said switch," where Switch 760 selects input to the ADC 720. A digital multiplexer (MUX) 780 is coupled to the ADC 720 to route the output therefrom… The ADCs, DACs and digital MUX 780 may reside on a separate

integrated circuit from the radio transceiver integrated circuit. For example, these components may reside on the baseband integrated circuit where a baseband demodulator 790…reside [¶ 0071, Fig. 11];

The '753 publication does not expressly disclose the sample-and-hold circuits being operable to extract a discrete value from an output signal from corresponding one of said plurality of receiver branches or a switch being operable to allow output signals from said plurality of sample-and-hold circuits to be selectively fed out of said switch at time intervals.

The '183 publication does expressly disclose " sample-and-hold circuits being operable to extract a discrete value from an output signal from corresponding one of said plurality of receiver branches," where a sample/hold (S/H) circuit 212(i) is coupled to the input of the ADC 210(i). A control circuit or logic 230 generates control signals to control the S/H circuits 212(i) [¶ 0032, Fig. 3];

The '183 publication further discloses "a switch being operable to allow output signals from said plurality of sample-and-hold circuits to be selectively fed out of said switch at time intervals," where the multiplexer 170 comprises receiver multiplexer circuits 170(3) and 170(4) that route the receive signals produced by the radio IC 150. Similar to FIGS. 6 and 7, the timing blocks 240 and 160 coordinate the exchange of signals according to the timing pattern shown in FIG. 9. For example, during a first time interval multiplexer 170(3) routes to receiver connection pins 5 and 6, respectively, Rx DataI1+ and Rx DataI1- from S/H

circuit 159(5) and subsequently during a second time interval routes to receiver connection pins 5 and 6, respectively, Rx DataQ1+ and Rx DataQ1- from SH circuit 159(6). Similarly, during the first time interval multiplexer 170(4) routes to receiver connection pins 7 and 8, respectively, Rx DataI2+ and Rx DataI2- from S/H circuit 159(7) and subsequently during a second time interval routes to receiver connection pins 7 and 8, respectively, Rx DataQ2+ and Rx DataQ2- from S/H circuit 159(8). Thus, the receiver multiplexer circuits couple during different time intervals (e.g., alternately couple) receive I and Q signals to the corresponding receiver connection pin from the I and Q signal paths, respectively, of the receiver in the radio IC [¶ 0040, Fig. 9].

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the receiver of the '753 publication with the sample-and-hold and switch of the "'183 publication. The suggestion/motivation would have been in order to use a minimum number of pins, and supporting circuitry that does not unduly add to the silicon area, power consumption and development risk to the radio IC [¶ 0004].

As to Claim 2, the '753 and '183 publications disclose a receiver as recited in Claim 1.

The '753 publication further discloses "wherein each of said receiver branches includes a band pass filter operable to allow corresponding one of the signals to travel through a certain band, and a first amplifier operable to amplify an output signal from said band pass filter," where each branch in the receiver

circuits 140 and 170 is coupled to a corresponding one of the bandpass filters 120, 122, 124 or 126 in the RF front end section 105 shown in FIG. 5. In a first branch of the receiver circuit 140, there is a low noise amplifier (LNA) 142 and an RF mixer 144 to downconvert an RF signal from a first radio frequency band (RFB1) to an intermediate frequency (IF). In a second branch of the receiver circuit 140 there is an LNA 152 and an RF mixer 154 that downconverts an RF signal from a second radio frequency band to IF…the first branch of receiver circuit 140 (consisting of LNA 142 and mixer 144) processes a signal from a first RF band (RFB1) detected by antenna 102. The second branch of receiver circuit 140 (consisting of amplifier 152 and mixer 154) processes a signal from a second RF band (RFB2) detected by antenna 102 [¶ 0039, Fig. 5].

As to Claim 3, the '753 and '183 publications disclose a receiver as recited in Claim 2.

The '753 publication further discloses "wherein each of said receiver branches includes an antenna," where the radio transceiver provides, on a single semiconductor integrated circuit, a receiver circuit or path for each of a plurality of antennas and a transmit circuit or path for each of the plurality of antennas [¶ 0011].

As to Claim 4, the '753 and '183 publications disclose a receiver as recited in Claim 1.

The '753 publication further discloses "an analog-to-digital converter connected between said switch and said demodulating unit, said analog-to-digital

converter being operable to convert the output signals from said switch in value from analog values to digital values," where a digital multiplexer (MUX) 780 is coupled to the ADC 720 to route the output therefrom, and to the DAC 730 to coordinate input thereto. The ADCs, DACs and digital MUX 780 may reside on a separate integrated circuit from the radio transceiver integrated circuit. For example, these components may reside on the baseband integrated circuit where a baseband demodulator 790 and a baseband modulator 795 reside [¶ 0071] and further discloses that switches 200 and 202 are coupled to the sample-and-hold circuits in receiver circuits 140 and 170, respectively, to switch between the I and Q outputs associated with the first and second analog baseband receive signals output by receiver circuit 140 and receiver circuit 170, respectively, for processing by an ADC [¶ 0041] where the ADC [analog-to-digital converter] being operable to convert signals from analog to digital values is an obvious variation of the claimed invention.

As to Claim 5, the '753 and '183 publications disclose a receiver as recited in Claim 4.

The '753 publication further discloses "a clock-generating unit operable to generate clock signals to be fed into said plurality of sample-and-hold circuits, said switch, and said analog-to-digital converter," where an interface and control block 290 interfaces a clock signal, data signals and an enable signal to/from an external device, such as a baseband processor and/or a control processor. Transceiver control signals sourced from an external device may be coupled to

the appropriate transceiver components through the interface control block 290 or coupled to pins that are tied to the appropriate components…The switch control signals control the position of the switches 106, 108, 110, 112, 114, 116, 200 and 202 according to the operating mode of the radio transceiver 100 and the frequency band of operation [¶ 0046] where the transceiver control signals would be operable to control any desired characteristic of the transceiver that employs a sample-and-hold circuit, switch or analog-to-digital converter.

As to Claim 6, the '753 and '183 publications disclose a receiver as recited in Claim 5.

The '753 publication further discloses "an amplifier connected to said clock-generating unit, said amplifier being operable to amplify the clock signals from said clock-generating unit by an integer multiple comparable in number to said plurality of receiver branches," where a dual modulus phase-lock loop (PLL) 430, VCOs 432, 434 and 436, a squaring block 438…may be provided to supply the appropriate in-phase and quadrature RF local oscillator signals to the mixers 320 and 322, respectively, in receiver circuit 310…the dual modulus 430 is a standard component for generating high frequency signals. The squaring block 438 acts as a frequency doubler, reducing the pull of the VCO by the power amplifiers [¶ 0060] and further discloses that the RF local oscillator signal output of the RF LO synthesizer 260 is coupled to a divide-by-four circuit 265 which in turn supplies an IF local oscillator signal to mixers 148 and 156 in receiver circuit

140 [¶ 0053] where the PLL and squaring block operate to amplify the local oscillator signals by an integer multiple (i.e. divide-by-four);

The '753 publication discloses "an output from said amplifier is fed into said switch and said analog-to-digital converter," where in the receiver circuit 310, there are two amplifiers 312 and 314 both coupled to a switch 316. Amplifier 312 receives a bandpass filtered signal in frequency band RFB1 from a bandpass filter in the RF front end section 105 (FIG. 2), and similarly amplifier 314 receives a bandpass filtered signal in frequency band RFB2. The output of the switch 316 is coupled to a variable amplifier 318 to adjust the gain of the signal supplied to its input. The output of the variable amplifier 318 is coupled to mixers 320 and 322 that down-mix the amplified receive signal by IF local oscillator signals to produce I and Q signals…A switch 336 is controlled to alternately select between the baseband I and Q signals for coupling to a single ADC, saving the cost of a second ADC[¶ 0055, Figs. 2 and 4].

As to Claim 7, the '753 and '183 publications disclose a receiver as recited in Claim 4.

The '753 publication discloses "a second amplifier connected to said analog-to-digital converter at an input of said analog-to-digital converter," where a switch 336 is controlled to alternately select between the baseband I and Q signals for coupling to a single ADC [¶ 0055];

The '753 publication further discloses "a gain control unit operable to control a gain in said second amplifier; and a gain control information-detecting

unit operable to detect gain control information to be fed into said gain control unit," where an interface and control block 290 interfaces a clock signal, data signals and an enable signal to/from an external device, such as a baseband processor and/or a control processor…the receive gain control signals control the gain of the variable amplifiers 146 and 176 on the receive side [¶ 0046] where the interface and control block feeds information regarding receiver gain to the transceiver for processing.

As to Claim 11, the '753 and '183 publications disclose a receiver as recited in Claim 4.

The '753 publication further discloses "a plurality of third amplifiers, each of which is connected to corresponding one of said plurality of sample-and-hold circuits, each of said plurality of third amplifiers being operable to amplify an output from corresponding one of said plurality of sample-and-hold circuits," where outputs of the sample-and-hold circuits 372 and 374 are coupled to the variable lowpass filters 376 and 378. The outputs of the lowpass filters 376 and 378 are coupled to quad mixers 380 and 382, respectively. The quad mixers 380 and 382 up-mix the filtered I and Q signals output by the lowpass filters 376 and 378 to output RF I and Q signals which are combined and coupled to a variable amplifier 384. The variable amplifier 384 adjusts the gain of the first RF signal and supplies this signal to bandpass filters 386 and 388, respectively. The outputs of bandpass filters 386 and 388 are coupled to power amplifier 394 and 396. Power amplifiers 390 and 392 amplify the RF signals for frequency bands

RFB1 and RFB2 which are coupled to the RF front end 105 [¶ 0058] where the RF front end illustrated in Fig. 5 is passed on to a corresponding receiving antenna.

The ‘753 publication discloses "a gain control unit operable to control gains in said plurality of third amplifiers" as recited in the rejection of Claim 7, incorporating an additional amplifier would be an obvious variation.

The ‘753 publication discloses "a gain control information-detecting unit operable to detect gain control information to be fed into said gain control unit " as recited in the rejection of Claim 7.

As to Claim 14, the ‘753 and ‘183 publications disclose a receiver as recited in Claim 5.

The ‘753 publication does not expressly disclose a clock control unit operable to control a clock frequency in said clock-generating unit.

The ‘183 publication does expressly disclose “a clock control unit operable to control a clock frequency in said clock-generating unit,” where a timing control block 240 is provided in the baseband IC 200 and a timing control block 160 is provided in the radio IC 150. The timing blocks are driven off of an external clock reference, and the clock signals synchronize clcok+ (SCLP) and synchronize clock- (SCLN) generated in either the baseband IC 200 or radio IC 150 to coordinate the exchange of signals according to the timing pattern shown in Fig. 7 [¶ 0038] and further discloses that similar to Figs. 6 and 7, the timing blocks

240 and 160 coordinate the exchange of signals according to the timing pattern shown in Fig. 9 [¶ 0040, Figs. 8 and 9].

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the receiver of the '753 publication with the clock control unit of the '183 publcation. The suggestion/motivation would have been in order to couple the receiver mutiplexer circuits during different time intervals ['183 publication, ¶ 0040].

As to Claim 15, the '753 and '183 publications disclose a receiver as recited in Claim 14.

The '753 publication does not expressly disclose a clock control unit operable to divide the clock frequency in said clock-generating unit in accordance with a number of frequency division multiplex signals in operative use when the signals received by said plurality of receiver branches include the frequency division multiplex signals.

The '183 publication does expressly disclose "a clock control unit operable to divide the clock frequency in said clock-generating unit in accordance with a number of frequency division multiplex signals in operative use when the signals received by said plurality of receiver branches include the frequency division multiplex signals," where The timing blocks are driven off of an external clock reference, and the clock signals synchronize clcok+ (SCLP) and synchronize clock- (SCLN) generated in either the baseband IC 200 or radio IC 150 to coordinate the exchange of signals according to the timing pattern shown in Fig.

7 [¶ 0038] where the corresponding receiver is illustrated in Figure 9. Figure 9 depicts a four cycle reference clock divided into four frequency division multiplex signals for each receiver branch (Rx Data 1+ and Rx Data 2+). In addition, the same motivation is used as in the rejection of Claim 14.

Claim 19 is drawn to similar limitations recited in Claims 1, 4, 5 and 14. Therefore, Claim 19 is rejected for the same reasons set forth in the rejections of Claims 1, 4, 5 and 14.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0121753 to Sugar et al ('753 publication) and in view of U.S. Patent Publication 2004/0242183 to Sugar et al ('183 publication) as applied to Claim 1 above and in further view of U.S. Patent Publication 2004/0125900 to Liu et al ("Liu").

As to Claim 8, the '753 and '183 publications disclose a receiver as recited in Claim 7.

The '753 and '183 publications do not expressly disclose that the gain control information is a signal-to-noise ratio detected by said demodulating unit.

Liu does expressly disclose that "the gain control information is a signal-to-noise ratio detected by said demodulating unit," where capacity calculator 118 separately calculates the capacity of each of the t transmitter antennas 109 from the measured channel coefficients in the H matrix determined by channel estimator 114, the known number of transmitter antennas, t, and the measured signal-to-noise ratio, ρ. S/N detector 120, connected to the output of RF

demodulators 112-1-112-r, determines the latter. The t calculated antenna transmitter capacities are then fed back to the transmitter end 101 [¶ 0024] and further discloses that The t combined RF-frequency signals received by each of the r receiver antennas 111-1-111-r are down-converted to baseband signals by demodulators 112-1-112-r, respectively. A data processor 113 processes the resultant r baseband signals and converts them back into t data streams, corresponding to the t data streams at the outputs of modulators 107-1-107-t. Data processor 113 uses an r-by-t instantaneous channel response matrix H, the coefficients of which are determined by channel estimator 114 from the r baseband signals, to transform the r base-band signals into t output data streams [¶ 0013].

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the receiver of the '753 and '183 publications with the gain control information of Liu. The suggestion/motivation would have been in order to determine the per antenna capacity of each transmitter antenna individually at the receiver end [¶ 0004].

As to Claim 9, the '753 and '183 publications disclose a receiver as recited in Claim 7.

The '753 and '183 publications do not expressly disclose that the gain control information is a bit error rate detected by said demodulating unit.

Liu does expressly disclose that "the gain control information is a bit error rate detected by said demodulating unit," where the per antenna capacity of each

of the transmitter antennas in a MIMO system are individually determined from measurable information at the receiver end. Specifically, it has been determined that the channel capacity for each individual transmitter antenna can be calculated at the receiver end as a function of measurable channel coefficients (also known as channel state information) [¶ 0004] and further discloses capacity calculator 118 separately calculates the capacity of each of the t transmitter antennas 109 from the measured channel coefficients in the H matrix determined by channel estimator 114, the known number of transmitter antennas, t, …connected to the outputs of RF demodulators 112-1-112-r… the rate and modulation selector 108 uses the t fed back transmitter capacities to determine for each transmitter antenna 109, an optimum data rate and modulation and coding scheme to maintain the usage of each transmitter antenna below its determined capacity…the rate and modulation selector 108 could alternatively be at the receiver end 102 either incorporated as part of the capacity calculator 118, or as a separate element [¶ 0024-0026]. In addition, the same motivation is used as in the rejection of Claim 8.

6. Claims 10, 12, 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0121753 to Sugar et al ('753 publication) and in view of U.S. Patent Publication 2004/0242183 to Sugar et al ('183 publication) as applied to Claim 1 above and in further view of U.S. Patent 7,333,788 to Eilts al ("Eilts").

As to Claim 10, the '753 and '183 publications disclose a receiver as recited in Claim 7.

The '753 and '183 publications do not expressly disclose that a second amplifier has an amplification degree within a dynamic range of said analog-to-digital converter.

Eilts does expressly disclose that "a second amplifier has an amplification degree within a dynamic range of said analog-to-digital converter," where each digital output from the 10-bit ADC would be the number between from 0 to 1023 that represents the binary value that most closely matches the actual input voltage. It is axiomatic that the converting an analog signal to digital samples introduces a small amount of error, i.e., the difference between the actual input voltage and the closest voltage having a binary representation. To minimize the effect of these errors, it is desirable to match the range of the analog input voltages to the maximum range of the ADC. Thus, the maximum expected analog input voltage should convert to a value near the maximum representable by the ADC, and the minimum expected analog input voltage should convert to a value near the minimum representable by the ADC…the receiving transceiver 104B may attempt to apply inappropriate gains to certain incoming data signals. providing a signal size exceeding the limits of internal hardware components or the ADCs 146 and 148 and resulting in severe signal distortion…The AGC controller 154 may correct for such a problem by adjusting the receiving

transceiver 104B gain, thereby keeping the data signal input into the ADCs 146 and 148 at an appropriate size [Col. 4, lines 40 – 53; Col. 5, lines 8-21].

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the receiver of the '753 and '183 publications with the amplifier of Eilts. The suggestion/motivation would have been in order to periodically measure the effects of the gain settings to permit accurate compensation in the receiver chain [Eilts, Col. 4, lines 9-11].

As to Claim 12, the '753 and '183 publications disclose a receiver as recited in Claim 11.

The '753 and '183 publications do not expressly disclose wherein each of said plurality of third amplifiers has substantially identical gain characteristic.

Eilts does expressly disclose that "each of said plurality of third amplifiers has substantially identical gain characteristic," where the AGC controller 154 may correct for such a problem by adjusting the receiving transceiver 104B gain, thereby keeping the data signal input into the ADCs 146 and 148 at an appropriate size [Col. 5, lines 18-21] and further discloses that the AGC controller 154 may also receive commands from the processor 150 to set the gain settings to fixed values or to increment/decrement the gain settings [Col. 5, lines 34-37].

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the receiver of the '753 and '183 publications with the amplifier of Eilts. The suggestion/motivation would have been in order to keep

the data signal input into the ADCs at an appropriate size [Eilts, Col. 5, lines 20-21].

Claim 13 is drawn to similar limitations as claimed in Claims 10 and 11. In regards to the limitation citing that a highest gain possessed by one of output signals from said plurality of sample-and-hold circuits to be amplified, it is addressed in the rejection of Claim 10. Eilts discloses in order to reduce errors at the ADC, it is desirable to match the range of the analog input voltages to the maximum range of the ADC. Thus, the maximum expected analog input voltage should convert to a value near the maximum representable by the ADC [Col. 4, lines 47-51]. In addition, the same motivation is used as in the rejection of Claim 12.

Claim 18 is drawn to similar limitations recited in Claims 1, 4, 7, 10 and 11. Therefore, Claim 18 is rejected for the same reasons set forth in the rejections of Claims 1, 4, 7, 10 and 11.

7. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0121753 to Sugar et al ('753 publication) and in view of U.S. Patent Publication 2004/0242183 to Sugar et al ('183 publication) as applied to Claim 1 above and in further view of U.S. Patent Publication 2001/0013075 to Otsaka et al ("Otsaka").

As to Claim 16, the '753 and '183 publication discloses a receiver as recited in Claim 1.

The ‘753 and ‘183 publications do not expressly disclose wherein a length of wiring extending from an input end of each of said plurality of receiver branches to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches include the frequency division multiplex signals.

Otsaka does expressly disclose “a length of wiring extending from an input end of each of said plurality of receiver branches to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches include the frequency division multiplex signals,” where the signal transmission line pair 1 comprises two parallel signal transmission lines 1a, 1b of equal length [Col. 11, lines 8-9] where the plurality of receiver branches to each of said sample-and-hold circuits is disclosed in the rejection cited in the ‘753 and ‘183 publications of Claim 1. Further, it includes the frequency division multiplex signals in the rejections cited in the ‘183 publication of Claim 15.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the receiver of ‘753 and ‘183 publications with the wiring length described by Otsaka. The suggestion/motivation would have been in order to suppress electromagnetic interference [Col. 11, line 44].

As to Claim 17, the ‘753 and ‘183 publication discloses a receiver as recited in Claim 1.

The ‘753 and ‘183 publications do not expressly disclose wherein a load of wiring extending from an input end of each of said plurality of receiver branches

to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches include the frequency division multiplex signals.

Otsaka does expressly disclose "a load of wiring extending from an input end of each of said plurality of receiver branches to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches include the frequency division multiplex signals," where the termination resistance 2, which terminates one end of the signal transmission line pair 1, is matched to the characteristic impedance of the signal transmission lines 1a, 1b [Col. 11, lines 9-12]. In addition, the same motivation is used as in the rejection of Claim 16.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EBONI GILES whose telephone number is (571)270-7453. The examiner can normally be reached on 7:30 AM - 5 PM, M-F, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Abul Azad can be reached on (571) 272-7599. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABUL AZAD/
Supervisory Patent Examiner, Art Unit 4133

/EBONI GILES/
Examiner, Art Unit 4133